FLEX 10K
On-Chip RAM Efficiency

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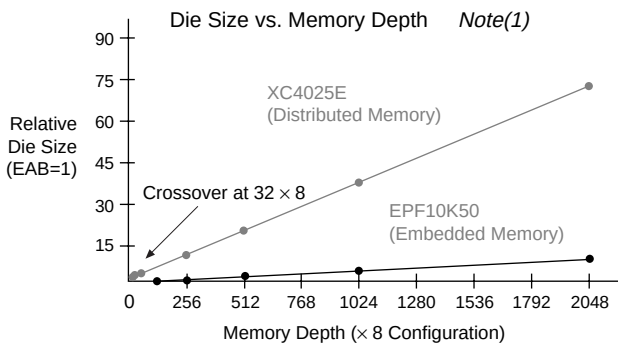
In the past, programmable logic devices (PLDs) have not been able to implement RAM without wasting logic resources. For example, FPGA RAM blocks are distributed across an entire device. Connecting these small blocks to form larger, usable RAM blocks requires additional logic. Consequently, RAM-intensive applications that are implemented with FPGAs, such as Xilinx XC4000E devices, use silicon inefficiently and perform poorly.

In contrast, the FLEX 10K architecture efficiently integrates memory and logic in a single device. FLEX 10K devices have dedicated blocks of embedded programmable memory bits, called embedded array blocks (EABs), which implement on-chip RAM blocks that are larger, use less area, and perform better than those of FPGAs.

Embedded RAM: A More Efficient Approach

As memory depth increases, the die size of a device that uses distributed RAM blocks increases far more rapidly than that of a device that uses embedded RAM. With embedded RAM, more RAM can be implemented in a device without a significant increase in die size, resulting in lower device costs.



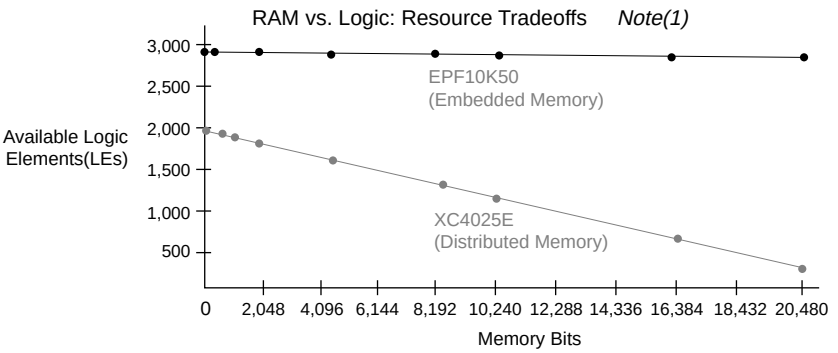
Notes:
(1) The data was compiled by Altera Applications.

RAM vs. Logic Tradeoffs

FLEX 10K EABs are separate from the logic array and are designed to implement RAM and other logic functions without decreasing the device logic capacity. In contrast, the logic capacity of the XC4025E decreases significantly as RAM requirements increase because XC4000E family RAM is created by converting CLBs into blocks of 32-bit RAM. For each CLB converted to RAM, the device has one less CLB for logic.

Embedded RAM Uses Less Silicon

Each FLEX 10K EAB provides 2 Kbits of RAM, whereas XC4000E CLBs provide only 32 bits of RAM. Building larger memory blocks in XC4000E devices not only consumes logic resources (i.e., CLBs) for the RAM itself as well as for decoding circuits, but also depletes routing resources.



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In addition, XC4000E devices require built-in synchronization circuitry for every 16 bits of RAM. Consequently, implementing a 2-Kbit block of RAM requires 128 copies of the same synchronization circuit. Additionally, when a CLB is used for logic, the memory write synchronization circuitry still exists in silicon, even though it serves no purpose. For the same 2 Kbits of RAM, FLEX 10K devices require only a single synchronization circuit.

Conclusion

The FLEX 10K family offers densities of up to 100,000 gates and provides an efficient way to implement on-chip RAM. Together, density and efficiency allow designers to incorporate more logic and memory into one device, making it possible to implement entire subsystems on a single chip.

The documents listed below provide more detailed information. Part numbers are in parentheses.

Product Information Bulletins

- *PIB 20: Benefits of Embedded RAM in FLEX 10K Devices* (A-PIB-020-01)
- *PIB 21: Designing with the Embedded Array in FLEX 10K Devices* (A-PIB-021-01)

Application Notes

- *AN 52: RAM Functions in FLEX 10K Devices* (A-AN-052-01)
- *AN 69: Implementing Register Files in FLEX 10K Devices* (A-AN-069-01)

You can request them from:

- Altera Express fax service at (800) 5-ALTERA
- World-Wide Web at **http://www.altera.com**
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